Refine Search

Search Results -

Terms	Documents
L2 AND (bit-field OR (bit ADJ field))	8

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L4

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Saturday, September 18, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=NO; OP=OR			
L4	L2 AND (bit-field OR (bit ADJ field))	8	L4
L3	L2 AND define	63	L3
L2	L1 AND declarative	68	L2
L1	MACRO AND bit	6178	L1

END OF SEARCH HISTORY

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 8 of 8 returned.

☐ 1. Document ID: US 6701338 B2

L4: Entry 1 of 8 File: USPT Mar 2, 2004

US-PAT-NO: 6701338
DOCUMENT-IDENTIFIER: US 6701338 B2
** See image for Certificate of Correction **

TITLE: Cumulative status of arithmetic operations

DATE-ISSUED: March 2, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Narad; Charles E.	Santa Clara	CA		
Fall; Kevin	Berkley	CA		
MacAvoy; Neil	Redwood City	CA		
Shankar; Pradip	Fremont	CA		
Rand; Leonard M.	San Francisco	CA		
Hall; Jerry J.	Santa Clara	CA		

US-CL-CURRENT: 708/525; 709/223

ABSTRACT:

The present invention relates to a general-purpose programmable packet-processing platform for accelerating network infrastructure applications which have been structured so as to separate the stages of classification and action. Network packet classification, execution of actions upon those packets, management of buffer flow, encryption services, and management of Network Interface Controllers are accelerated through the use of a multiplicity of specialized modules. A language interface is defined for specifying both stateless and stateful classification of packets and to associate actions with classification results in order to efficiently utilize these specialized modules.

64 Claims, 19 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 19

Full | Title | Citation | Front | Review | Classification | Date | Reference | [illegible] | Claims | KWIC | Draw. De

☐ 2. Document ID: US 6625689 B2

L4: Entry 2 of 8 File: USPT Sep 23, 2003

US-PAT-NO: 6625689
DOCUMENT-IDENTIFIER: US 6625689 B2
** See image for Certificate of Correction **

TITLE: Multiple consumer-multiple producer rings

DATE-ISSUED: September 23, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Narad; Charles E.	Santa Clara	CA		
Fall; Kevin	Berkley	CA		
MacAvoy; Neil	Redwood City	CA		
Shankar; Pradip	Fremont	CA		
Rand; Leonard M.	San Francisco	CA		
Hall; Jerry J.	Santa Clara	CA		

US-CL-CURRENT: 711/110

ABSTRACT:

The present invention relates to a general-purpose programmable packet-processing platform for accelerating network infrastructure applications which have been structured so as to separate the stages of classification and action. Network packet classification, execution of actions upon those packets, management of buffer flow, encryption services, and management of Network Interface Controllers are accelerated through the use of a multiplicity of specialized modules. A language interface is defined for specifying both stateless and stateful classification of packets and to associate actions with classification results in order to efficiently utilize these specialized modules.

145 Claims, 19 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 19

Full | Title | Citation | Front | Review | Classification | Date | Reference | [illegible] | Claims | KWMC | Draw De

---

☐ 3. Document ID: US 6421730 B1

L4: Entry 3 of 8 File: USPT Jul 16, 2002

US-PAT-NO: 6421730
DOCUMENT-IDENTIFIER: US 6421730 B1

TITLE: Programmable system for processing a partitioned network infrastructure

DATE-ISSUED: July 16, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Narad; Charles E.	Santa Clara	CA		
Fall; Kevin	Berkley	CA		
MacAvoy; Neil	Redwood City	CA		
Shankar; Pradip	Fremont	CA		
Rand; Leonard M.	San Francisco	CA		
Hall; Jerry J.	Santa Clara	CA		

US-CL-CURRENT: 709/236

ABSTRACT:

The present invention relates to a general-purpose programmable packet-processing platform for accelerating network infrastructure applications which have been structured so as to separate the stages of classification and action. Network packet classification, execution of actions upon those packets, management of buffer flow, encryption services, and management of Network Interface Controllers are accelerated through the use of a multiplicity of specialized modules. A language interface is defined for specifying both stateless and stateful classification of packets and to associate actions with classification results in order to efficiently utilize these specialized modules.

54 Claims, 19 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 19

☐ 4. Document ID: US 6401117 B1

L4: Entry 4 of 8 File: USPT Jun 4, 2002

US-PAT-NO: 6401117
DOCUMENT-IDENTIFIER: US 6401117 B1
**** See image for Certificate of Correction ****

TITLE: Platform permitting execution of multiple network infrastructure applications

DATE-ISSUED: June 4, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Narad; Charles E.	Santa Clara	CA		
Fall; Kevin	Berkley	CA		
MacAvoy; Neil	Redwood City	CA		
Shankar; Pradip	Fremont	CA		
Rand; Leonard M.	San Francisco	CA		
Hall; Jerry J.	Santa Clara	CA		

US-CL-CURRENT: 709/223

ABSTRACT:

The present invention relates to a general-purpose programmable packet-processing platform for accelerating network infrastructure applications which have been structured so as to separate the stages of classification and action. Network packet classification, execution of actions upon those packets, management of buffer flow, encryption services, and management of Network Interface Controllers are accelerated through the use of a multiplicity of specialized modules. A language interface is defined for specifying both stateless and stateful classification of packets and to associate actions with classification results in order to efficiently utilize these specialized modules.

36 Claims, 19 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 19

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWMC | Draw De

---

☐ 5. Document ID: US 6157955 A

L4: Entry 5 of 8 File: USPT Dec 5, 2000

US-PAT-NO: 6157955
DOCUMENT-IDENTIFIER: US 6157955 A
**** See image for Certificate of Correction ****

TITLE: Packet processing system including a policy engine having a classification unit

DATE-ISSUED: December 5, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Narad; Charles E.	Santa Clara	CA		
Fall; Kevin	Berkley	CA		
MacAvoy; Neil	Redwood City	CA		
Shankar; Pradip	Fremont	CA		
Rand; Leonard M.	San Francisco	CA		
Hall; Jerry J.	Santa Clara	CA		

US-CL-CURRENT: 709/228

ABSTRACT:

The present invention relates to a general-purpose programmable packet-processing platform for accelerating network infrastructure applications which have been structured so as to separate the stages of classification and action. Network packet classification, execution of actions upon those packets, management of buffer flow, encryption services, and management of Network Interface Controllers are accelerated through the use of a multiplicity of specialized modules. A language interface is defined for specifying both stateless and stateful classification of packets and to associate actions with classification results in order to efficiently utilize these specialized modules.

26 Claims, 19 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 19

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

---

☐ 6. Document ID: US 5680585 A

L4: Entry 6 of 8 File: USPT Oct 21, 1997

US-PAT-NO: 5680585
DOCUMENT-IDENTIFIER: US 5680585 A

TITLE: Method and apparatus for defining data packet formats

DATE-ISSUED: October 21, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bruell; Gregory O.	Carlisle	MA		

US-CL-CURRENT: 703/26

ABSTRACT:

A packet description language which is declarative in nature and suitable for efficiently and flexibly defining data packet formats in accordance with internetwork routing device uses. Data packet formats may be defined utilizing the packet description language and then compiled to create a data structure corresponding to the defined data packet format. A routing device test platform may generate test data packets and decode received test packets by referencing the test data to the compiled data structure defined in accordance with the packet description language. The declarative language provides for assigning numerous default values and attributes to packet fields such that only a small amount of data need be specified when regression testing a new routing device.

14 Claims, 5 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 4

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

---

☐ 7. Document ID: US 4791550 A

L4: Entry 7 of 8 File: USPT Dec 13, 1988

US-PAT-NO: 4791550
DOCUMENT-IDENTIFIER: US 4791550 A

TITLE: Higher order language-directed computer

DATE-ISSUED: December 13, 1988

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Stevenson; David R.	Los Altos Hills	CA		
Devlin; Michael T.	Sunnyvale	CA		

US-CL-CURRENT: 718/106; 707/4

ABSTRACT:

A higher order language-directed computer architecture particularly adaptable for fourth generation program languages. The computer includes a memory which stores package modules and task modules for programs, each of which includes a control segment representing control for the module, a code segment representing instructions for the computer relating to the module, a data segment, a type segment representing type descriptors declared for the module, a queue segment containing synchronization messages for controlling queuing between task modules and an import segment containing lists of objects outside a module which are accessible within the module. The computer simultaneously manipulates portions of the segments based on instructions in the code segment.

19 Claims, 19 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 18

☐ 8. Document ID: US 4667290 A

L4: Entry 8 of 8 File: USPT May 19, 1987

US-PAT-NO: 4667290
DOCUMENT-IDENTIFIER: US 4667290 A

TITLE: Compilers using a universal intermediate language

DATE-ISSUED: May 19, 1987

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Goss; Clinton	New York	NY		
Rosenberg; Richard	Brooklyn	NY		
Whyte; Peter	Fort Lee	NJ		

US-CL-CURRENT: 717/147; 713/1, 717/114, 717/143

ABSTRACT:

A method for directing a digital data processor to translate a program written in a source language into a sequence of machine executable instructions. The method consists of the translation of the source code into an intermediate language,

followed by generation of object code for the target machine, the method being generally applicable to known source languages and to digital data processors.

40 Claims, 2 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 2

Terms	Documents
L2 AND (bit-field OR (bit ADJ field))	8

Terms used **MACRO directive bit field definition** Found **42,583** of **142,346**

Sort results by relevance

Display results expanded form

Save results to a Binder

Search Tips

Open results in a new window

Try an Advanced Search

Try this search in The ACM Guide

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next

Best 200 shown Relevance scale

1 Diagrammatic function description of microprocessor and data-flow processor

Gotaro Odawara, Masahiro Tomita, Ichiro Ogata

June 1985 **Proceedings of the 22nd ACM/IEEE conference on Design automation**

Full text available: pdf(416.19 KB) Additional Information: full citation, abstract, references, index terms

This paper discusses a description technique for various kinds of processors. This technique is based on the Symbolic Functional Description Language, which allows logic designers to describe the behavior of hardwares at the register-transfer level in the top-down approach. The SFDL has been applied to the description of the internal behavior of a microprocessor and a data-flow processor. As a result, the SFDL has made it possible to describe the instruction set and the behavior ...

2 USC: a universal stub compiler

Sean O'Malley, Todd Proebsting, Allen Brady Montz

October 1994 **ACM SIGCOMM Computer Communication Review , Proceedings of the conference on Communications architectures, protocols and applications**, Volume 24 Issue 4

Full text available: pdf(1.23 MB) Additional Information: full citation, abstract, references, citings, index terms

USC is a new stub compiler that generates stubs that perform many data conversion operations. USC is flexible and can be used in situations where previously only manual code generation was possible. USC generated code is up to 20 times faster than code generated by traditional argument marshaling schemes such as ASN.1 and Sun XDR. This paper presents the design of USC and a comprehensive set of experiments that compares USC performance with the best manually generated code and traditional s ...

3 High-cost CFD on a low-cost cluster

Thomas Hauser, Timothy I. Mattox, Raymond P. LeBeau, Henry G. Dietz, P. George Huang

November 2000 **Proceedings of the 2000 ACM/IEEE conference on Supercomputing (CDROM)**

Full text available: pdf(4.00 MB) Publisher Site Additional Information: full citation, abstract, references, index terms

Direct numerical simulation of the Navier-Stokes equations (DNS) is an important technique for the future of computational fluid dynamics (CFD) in engineering applications. However, DNS requires massive computing resources. This paper presents a new approach for implementing high-cost DNS CFD using low-cost cluster hardware. After describing the DNS

CFD code DNSTool, the paper focuses on the techniques and tools that we have developed to customize the performance of a cluster ...

4 Comparison of the Programming Languages C and Pascal
Alan R. Feuer, Narain H. Gehani
January 1982 **ACM Computing Surveys (CSUR)**, Volume 14 Issue 1
Full text available: pdf(1.75 MB) Additional Information: full citation, references, citings, index terms

5 A high-speed message-driven communication architecture
J. Peterson, E. Chow, H. Madan
June 1988 **Proceedings of the 2nd international conference on Supercomputing**
Full text available: pdf(1.27 MB) Additional Information: full citation, abstract, references, citings, index terms

The performance of a message-passing multiple instruction multiple data (MIMD) concurrent computer depends in large part on the communication processing overhead. A high-speed communication architecture is proposed for a hypercube-type supercomputer to attain the specific goals of message-driven processing. These goals include: direct hardware execution of messages, queueing of messages (using various paradigms), adaptive message routing, and special local registers for fast context ...

6 Programming languages: Symbol manipulation in FORTRAN: SASP I subroutines
M. J. Bailey, M. P. Barnett, P. B. Burleson
June 1964 **Communications of the ACM**, Volume 7 Issue 6
Full text available: pdf(1.06 MB) Additional Information: full citation, abstract, references, citings

A set of subroutines for use in FORTRAN are described whose purpose is to synthesize output strings from (i) input strings which have been analysed by the SHADOW general syntactic analysis subroutine reported earlier, and/or (ii) packed BCD strings formed in any way. Function-type subroutines are included for intermediate manipulations, which are performed on the strings which are stored in an abbreviated internal representation. The automatic way in which an internal representation for each new ...

7 First-class data-type representations in SCHEMEXEROX
Norman Adams, Pavel Curtis, Mike Spreitzer
June 1993 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 1993 conference on Programming language design and implementation**, Volume 28 Issue 6
Full text available: pdf(860.49 KB) Additional Information: full citation, abstract, references, citings, index terms

In most programming language implementations, the compiler has detailed knowledge of the representations of and operations on primitive data typed and data-type constructors. In SCHEMEXEROX, this knowledge is almost entirely external to the compiler, in ordinary, procedural user code. The primitive representations and operations are embodied in first-class "representation types" that are constructed and implemented in an abstract and high-level fashion. Despite this abstractness ...

8 Automated proofs of object code for a widely used microprocessor
Robert S. Boyer, Yuan Yu
January 1996 **Journal of the ACM (JACM)**, Volume 43 Issue 1
Full text available: pdf(2.41 MB) Additional Information: full citation, references, citings, index terms, review

Keywords: Ada, Boyer-Moore logic, C, Common Lisp, MC68xxx, Nqthm, automated reasoning, formal methods, machine code, mechanical theorem proving, object code, program proving, program verification

9 Design of an optimizing, dynamically retargetable compiler for common Lisp

Rodney A. Brooks, David B. Posner, James L. McDonald, Jon L. White, Eric Benson, Richard P. Gabriel

August 1986 **Proceedings of the 1986 ACM conference on LISP and functional programming**

Full text available: pdf(1.13 MB) Additional Information: full citation, references, citings

10 PSL: A Portable LISP System

Martin L. Griss, Eric Benson, Gerald Q. Maguire

August 1982 **Proceedings of the 1982 ACM symposium on LISP and functional programming**

Full text available: pdf(773.17 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents the implementation strategy and current status of a new Portable LISP System, PSL, based upon STANDARD LISP. PSL is written entirely in itself and is compiled with an efficient LISP compiler with machine-oriented optimizations. A full PSL is currently running on a DECSystem-20 and a VAX, and a preliminary version runs on a Motorola MC68000. Versions for a CRAY-1 and an IBM-370 are planned.

11 Computer Communication Networks: Approaches, Objectives, and Performance Considerations

Stephen R. Kimbleton, G. Michael Schneider

September 1975 **ACM Computing Surveys (CSUR)**, Volume 7 Issue 3

Full text available: pdf(3.99 MB) Additional Information: full citation, references, citings, index terms

12 Refined types: highly differentiated type systems and their use in the design of intermediate languages

J. R. Rose

June 1988 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 1988 conference on Programming Language design and Implementation**, Volume 23 Issue 7

Full text available: pdf(1.23 MB) Additional Information: full citation, references, index terms

13 Disciplined C

Yves L. Noyelle

December 1995 **ACM SIGPLAN Notices**, Volume 30 Issue 12

Full text available: pdf(841.96 KB) Additional Information: full citation, abstract, index terms

Some proposals to render the C language a truly high level language are presented, as well as a program verifying that a given C program conforms to those proposals.

14 The SimpleScalar tool set, version 2.0

Doug Burger, Todd M. Austin

June 1997 **ACM SIGARCH Computer Architecture News**, Volume 25 Issue 3

Full text available: pdf(985.46 KB) Additional Information: full citation, abstract, citings, index terms

This document describes release 2.0 of the SimpleScalar tool set, a suite of free, publicly available simulation tools that offer both detailed and high-performance simulation of modern microprocessors. The new release offers more tools and capabilities, precompiled binaries, cleaner interfaces, better documentation, easier installation, improved portability, and higher performance. This paper contains a complete description of the tool set, including retrieval and installation instructions, a d ...

15 Associative and Parallel Processors

Kenneth J. Thurber, Leon D. Wald

December 1975 **ACM Computing Surveys (CSUR)**, Volume 7 Issue 4

Full text available: pdf(2.62 MB) Additional Information: full citation, references, citings, index terms

16 The evolution of the Sperry Univac 1100 series: a history, analysis, and projection

B. R. Borgerson, M. L. Hanson, P. A. Hartley

January 1978 **Communications of the ACM**, Volume 21 Issue 1

Full text available: pdf(1.89 MB) Additional Information: full citation, abstract, citings, index terms

The 1100 series systems are Sperry Univac's large-scale mainframe computer systems. Beginning with the 1107 in 1962, the 1100 series has progressed through a succession of eight compatible computer models to the latest system, the 1100/80, introduced in 1977. The 1100 series hardware architecture Is based on a 36-bit word, ones complement structure which obtains one operand from storage and one from a high-speed register, or two operands from high-speed registers. The 1100 Operating System ...

Keywords: 1100 computer series, computer architecture, data management systems, end user facilities, executive control software, multiprocessing, multiprogramming, operating system, programming languages

17 An experiment in high level language microprogramming and verification

David A. Patterson

October 1981 **Communications of the ACM**, Volume 24 Issue 10

Full text available: pdf(1.22 MB) Additional Information: full citation, abstract, references, citings, index terms

The STRUM system was created to apply software engineering techniques to microprogramming. It provides the tools that allow the microprogrammer to use high level language, structured programming, and formal program verification to create emulations for a horizontally microprogrammed computer. This system is evaluated in two parts: (1) High level microprogramming language design and its use in structured microprogramming; and (2) Verification of a large microprogram. Both parts of this evalu ...

Keywords: high level microprogramming languages, microprogramming, optimization, structured microprogramming, verification

18 OOPSLA onward! track: Routine run-time code generation

Sam Kamin

December 2003 **ACM SIGPLAN Notices**, Volume 38 Issue 12

Full text available: pdf(538.01 KB) Additional Information: full citation, abstract, references, index terms

Run-time code generation (RTCG) would be used routinely if application programmers had a facility with which they could easily create their own run-time code generators, because it

would offer benefits both in terms of the efficiency of the code that programmers would produce and the ease of producing it. Such a facility would necessarily have the following properties: it would not require that programmers know assembly language; programmers would have full control over the generated code; the c ...

Keywords: Java, run-time code generation

19 Onward papers: Routine run-time code generation

Sam Kamin

October 2003 **Companion of the 18th annual ACM SIGPLAN conference on Object-oriented programming, systems, languages, and applications**

Full text available: pdf(295.83 KB) Additional Information: full citation, abstract, references, index terms

Run-time code generation (RTCG) would be used routinely if application programmers had a facility with which they could easily create their own run-time code generators, because it would offer benefits both in terms of the efficiency of the code that programmers would produce and the ease of producing it. Such a facility would necessarily have the following properties: it would not require that programmers know assembly language; programmers would have full control over the generated code; the c ...

Keywords: Java, run-time code generation

20 RISCs vs. CISCs for Prolog: a case study

Gaetano Borriello, Andrew R. Cherenson, Peter B. Danzig, Michael N. Nelson

October 1987 **Proceedings of the second international conference on Architectual support for programming languages and operating systems**, Volume 15 , 22 , 21 Issue 5 , 10 , 4

Full text available: pdf(1.65 MB) Additional Information: full citation, abstract, citings, index terms

This paper compares the performance of executing compiled Prolog code on two different architectures under development at U. C. Berkeley. The first is the PLM, a special-purpose CISC architecture intended as a coprocessor for a host machine. The second is SPUR, a general-purpose RISC architecture that supports tagged data. Fourteen standard benchmark programs were run on both the PLM and SPUR simulators. The compiled code for SPUR was obtained by simple macro-expansion of PLM code generated by t ...

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next

Your search matched **2028** of **1071730** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enter new one in the text box.

macro Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

---

1 **Data-driven parallel production systems: a macro actor/token implementation**
Sohn, A.; Gaudiot, J.-L.;
Intelligent Control, 1990. Proceedings., 5th IEEE International Symposium on Sept. 1990
Pages:327 - 332 vol.1

[Abstract] [PDF Full-Text (508 KB)] **IEEE CNF**

---

2 **Application specific macro based synthesis**
Sundararaman, S.; Govindarajan, S.; Vemuri, R.;
VLSI Design, 2001. Fourteenth International Conference on , 3-7 Jan. 2001
Pages:317 - 324

[Abstract] [PDF Full-Text (588 KB)] **IEEE CNF**

---

3 **High-level software energy macro-modeling**
Tan, T.K.; Raghunathan, A.; Lakshminarayana, G.; Jha, N.K.;
Design Automation Conference, 2001. Proceedings , 18-22 June 2001
Pages:605 - 610

[Abstract] [PDF Full-Text (596 KB)] **IEEE CNF**

---

4 **Design for testability of mixed-mode ASICs**
Butler, I.C.; Taylor, D.; Hallam, P.;
Testing-the Gordian Knot of VLSI Design, IEE Colloquium on , 28 May 1993
Pages:9/1 - 9/5

[Abstract] [PDF Full-Text (184 KB)] **IEE CNF**

---

5 **Macro processing in object-oriented languages**
Chiba, S.;
Technology of Object-Oriented Languages, 1998. TOOLS 28. Proceedings , 23
Nov. 1998
Pages:113 - 126

[Abstract] [PDF Full-Text (644 KB)] **IEEE CNF**

---

6 **Macros by example in a graphical UIMS**
Olsen, D.R., Jr.; Dance, J.R.;
Computer Graphics and Applications, IEEE , Volume: 8 , Issue: 1 , Jan. 1988
Pages:68 - 78

[Abstract] [PDF Full-Text (968 KB)] **IEEE JNL**

---

7 **Hybrid position/force control of flexible-macro/rigid-micro manipul systems**
Yoshikawa, T.; Harada, K.; Matsumoto, A.;
Robotics and Automation, IEEE Transactions on , Volume: 12 , Issue: 4 , Aug 1996
Pages:633 - 640

[Abstract] [PDF Full-Text (780 KB)] **IEEE JNL**

---

8 **The practical engineer-fine-tuning memory macros using variable internal delays**
Gray, K.;
Spectrum, IEEE , Volume: 36 , Issue: 8 , Aug. 1999
Pages:44 - 49

[Abstract] [PDF Full-Text (580 KB)] **IEEE JNL**

---

9 **Symbolic macro test for DSP systems applied to a voice coder appli**
Steensma, J.; Vanhoof, B.; Cathoor, F.; de Man, H.;
VLSI Signal Processing, VI, 1993., [Workshop on] , 20-22 Oct. 1993
Pages:215 - 223

[Abstract] [PDF Full-Text (392 KB)] **IEEE CNF**

---

10 **Precision force control via macro/micro actuator for surface moun system**
Duk-Young Lee; Hyungsuck Cho;
Intelligent Robots and System, 2002. IEEE/RSJ International Conference on , Volume: 3 , 30 Sept.-5 Oct. 2002
Pages:2227 - 2232 vol.3

[Abstract] [PDF Full-Text (532 KB)] **IEEE CNF**

---

11 **Accurate power macro-modeling techniques for complex RTL circui**
Potlapally, N.R.; Raghunathan, A.; Lakshminarayana, G.; Hsiao, M.S.; Chakra S.T.;
VLSI Design, 2001. Fourteenth International Conference on , 3-7 Jan. 2001
Pages:235 - 241

[Abstract] [PDF Full-Text (644 KB)] **IEEE CNF**

12 **Outage probability of CDMA-TDD micro cells in a CDMA-FDD environment**
Haas, H.; Povey, G.J.R.;
Personal, Indoor and Mobile Radio Communications, 1998. The Ninth IEEE International Symposium on , Volume: 1 , 8-11 Sept. 1998
Pages:94 - 98 vol.1

[Abstract] [PDF Full-Text (508 KB)] **IEEE CNF**

13 **An embedded FeRAM macro cell for a smart card microcontroller**
Miwa, T.; Yamada, J.; Okamoto, Y.; Koike, H.; Toyoshima, H.; Hada, H.; Hay Y.; Okizaki, H.; Miyasaka, Y.; Kunio, T.; Miyamoto, H.; Gomi, T.; Kitajima, H.
Custom Integrated Circuits Conference, 1998., Proceedings of the IEEE 1998 14 May 1998
Pages:439 - 442

[Abstract] [PDF Full-Text (548 KB)] **IEEE CNF**

14 **A parametric DCT macro cell generator with a simulation model an accuracy report**
Ohki, M.; Nagai, T.; Aikawa, M.; Seno, K.;
VLSI Signal Processing, VIII, 1995. IEEE Signal Processing Society [Workshop on] , 16-18 Sept. 1995
Pages:441 - 450

[Abstract] [PDF Full-Text (476 KB)] **IEEE CNF**

15 **Control system design for macro/micro manipulator with applicati electrodischarge machining**
Narikiyo, T.; Nakane, H.; Akuta, T.; Mohri, N.; Saito, N.;
Intelligent Robots and Systems '94. 'Advanced Robotic Systems and the Real World', IROS '94. Proceedings of the IEEE/RSJ/GI International Conference on , Volume: 2 , 12-16 Sept. 1994
Pages:1454 - 1460 vol.2

[Abstract] [PDF Full-Text (328 KB)] **IEEE CNF**

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 2
25 26 27 28 29 30 31 32 33 34 Next

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search | Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting | No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ| Terms | Back to Top

Google Web Images Groups News Froogle more »
whitehall clifford macro Search Advanced Search Preferences

Web

Results **1** - **10** of about **81** for **whitehall clifford macro**. (**0.55** seconds)

Information Management Network
... is the expected impact of the **macro** economy and ... CARLTON GROUP Craig Medwick, Partner **CLIFFORD** CHANCE LLP ... Vice President GOLDMAN SACHS, **WHITEHALL** STREET FUNDS. ...
www.imn.org/2003/a457/index.shtml?p=agenda.html - 52k - Cached - Similar pages

[DOC] CONTENTS
File Format: Microsoft Word 97 - View as HTML
... This leads to the shorthand description of □**Whitehall**□ as applying to the UK ... aims to work with the Bank of England to provide stable **macro**-economic management ...
www.cabinet-office.gov.uk/cdg/skillsandqualifications/ publication/downloads/doc/fywaw_dec2002.doc - Similar pages

[PDF] CABINET OFFICE PREFACE SAM MITHA
File Format: PDF/Adobe Acrobat - View as HTML
... This leads to the shorthand description of "**Whitehall**" as applying to the Civil ... to work with the Bank of England to provide stable **macro**-economic management ...
www.cabinet-office.gov.uk/ civilservice/publications/whiteha1.pdf - Similar pages

Market reports, business information and market research from ...
... Ceramics, Robert Lee (London) Ltd, **Whitehall** Fabrications, Viking ... Scope Distribution, Leaker Direct, G **Clifford** Morris, Trent ... 4.4.3 **Macro**-Economic Influences 33. ...
www.the-list.co.uk/acatalog/am45022.html - 33k - Cached - Similar pages

Det Kongelige Bibliotek - Nyanskaffelser - juli/august 2002
... Foucault : savage identities / Michael **Clifford** New York ... to New Labour; **Whitehall's** managerial revolution ... steering the economy - **macro**-economic management from ...
www.kb.dk/formidl/fagweb/2002-acc/jul/ga.htm - 101k - Cached - Similar pages

[DOC] The organisation of central government departments: a history ...
File Format: Microsoft Word 6 - View as HTML
The organisation of central government departments: a history, 1964-1992. Data base use and specifications. General Introduction. How to use the data base. ...
www.nuff.ox.ac.uk/politics/**whitehall**/Inform.doc - Similar pages

The Bookshop, Inc. at antiqbook.com
... The Impact of **Macro** Social Systems on Ethnic Minorities in the United States. ... John Dene of Toronto: A Comedy of **Whitehall**. ... 154930: JONES, **CLIFFORD** ANTHONY. ...
www.antiqbook.com/boox/bks/books10000.shtml - 101k - Sep 16, 2004 - Cached - Similar pages

TranceWorks at antiqbook.com
... Making Miracles Happen 005807: SMITH, **CLIFFORD** - Historical Sketches ... ALLEN AND FRANK
B. **WHITEHALL** - Optimizing Quality in ... in Assembly Language : **Macro**-11 016782 ...
www.antiqbook.com/boox/tra/books16000.shtml - 101k - Cached - Similar pages

[PS] From Proceedings of the Ninth International Conference on Machine ...
File Format: Adobe PostScript - View as Text
... (The syntax "A ! B where P " indicates a **macro**; it expands ... Pazzani, **Clifford** Brunk, and Glenn Silverstein. ... MIT Press. (**Whitehall**, 1990) Bradley L. **Whitehall**. ...

www-2.cs.cmu.edu/~wcohen/postscript/ml-92.ps - Similar pages

EBM221A

... M., Harold C. Cash & **Clifford** E. Young ... growth, image, etc.); a brief **macro**-environment analysis ... International; "Anadin" over the counter, **Whitehall** Labs; "Anais ...

prosper.swansea.ac.uk/ebms/mods9900/ebm221a.htm - 42k - Cached - Similar pages

Gooooooooogle ▶

Result Page: 1 2 3 4 5 6 7 8 **Next**

whitehall clifford macro Search

Search within results | Language Tools | Search Tips | Dissatisfied? Help us improve

Google Home - Advertising Programs - Business Solutions - About Google

Refine Search

Search Results -

Terms	Documents
L3 AND directive	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L4

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Saturday, September 18, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=NO; OP=OR			
L4	L3 AND directive	0	L4
L3	L1 AND bit	4	L3
L2	L1 AND macro	0	L2
L1	frid-nielsen.in.	9	L1

END OF SEARCH HISTORY